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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,144	10/27/2003	Stephen J. Estrop	MS1-1679US	3277
22801	7590	01/11/2005	EXAMINER	
LEE & HAYES PLLC 421 W RIVERSIDE AVENUE SUITE 500 SPOKANE, WA 99201			HSU, JONI	
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DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/694,144	Applicant(s) ESTROP, STEPHEN J.	
	Examiner Joni Hsu	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/4/04</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 25 recites the limitations "the data processing module" and "the instructions".

There is insufficient antecedent basis for these limitations in the claim. Applicant is assumed to have meant "the graphics processing module" instead of "the data processing module".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-9, 11-22, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsén (US 20040054689A1) in view of Herrera (US006208350B1).

6. With regard to Claim 1, Salmonsén describes a method for processing video data, comprising receiving a principal video stream from a source [0104]; receiving a video sub-stream containing supplemental information associated with the principal video stream [0137]; performing an operation on the principal video stream [0104] and combining the principal video stream with the video sub-stream to produce processed data; and outputting the processed data [0181].

However, Salmonsén does not teach that the performing and the combining are performed in a single stage operation. However, Herrera describes performing an operation on the principal video stream and combining the principal video stream with the video sub-stream to produce processed data. Herrera also describes that the performing and the combining are performed in a single stage operation (14, Figure 1; Col. 2, line 39-Col. 3, line 19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsén so that the performing and the combining are

performed in a single stage operation as suggested by Herrera because performing a single stage operation instead of multiple stage operations inherently makes the processing faster.

7. With regard to Claim 2, Salmonsens describes that the performing of the operation comprises de-interlacing the principal video stream [0104].

8. With regard to Claim 3, Salmonsens describes that the performing of the operation comprises resizing the principal video stream [0104].

9. With regard to Claim 4, Salmonsens does not teach that the performing and the combining involve a single call to memory. However, Herrera describes that the performing and the combining are performed in a single stage operation, and the operation is performed on the inputted DVD data stream (14, Figure 1; Col. 2, line 39-Col. 3, line 19). The inputted DVD data stream was inherently retrieved by a single call to memory.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsens so that the performing and the combining involve a single call to memory as suggested by Herrera because performing a single call to memory instead of multiple calls to memory inherently makes the processing faster.

10. With regard to Claim 5, Salmonsens does not teach that the performing and the combining are performed in a YUV color space. However, Herrera describes that the performing and the combining are performed in a YUV color space (Col. 2, line 51-Col. 3, line 19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsens so that the performing and the combining are performed in a YUV color space as suggested by Herrera. Using a YUV color space is well-known in the art and widely used. Some advantages of using a YUV color space are that they remain compatible with black and white analog television, and the signal YUV can be easily manipulated to deliberately discard some information in order to reduce bandwidth. YUV is a versatile format which can easily be combined into other legacy video formats. Combining or modulating can be accomplished easily in low-cost circuitry. The advantages of using a YUV color space can be found in many publications, such as the Wikipedia free encyclopedia.

11. With regard to Claim 6, Salmonsens describes a step of forwarding instructions to a graphics processing module, the instructions informing the graphics processing module how to execute the performing and the combining (Figure 2) [0033, 0104, 0181].

12. With regard to Claim 7, Salmonsens does not teach that the instructions identify a location at which to receive the principal video stream, a location at which to receive the video sub-stream, and a location at which to provide the processed data. However, Herrera describes that the instructions identify a location at which to receive the principal video stream, a location at which to receive the video sub-stream, and a location at which to provide the processed data (Figure 7; Col. 13, lines 4-20; Col. 6, lines 12-20; Col. 15, lines 64-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsens so that the instructions identify a location at which

to receive the principal video stream, a location at which to receive the video sub-stream, and a location at which to provide the processed data as suggested by Herrera because Herrera suggests that the locations must be identified in the instructions so that the data will be sent to the correct destination (Figure 7; Col. 13, lines 4-20; Col. 6, lines 12-20; Col. 15, lines 64-67).

13. With regard to Claim 8, Salmonsens does not teach that the instructions identify a rectangle of data from which to receive the principal video stream within a video stream surface, a rectangle of data from which to receive the video sub-stream within a video sub-stream surface, and a rectangle at which to output the processed data within a destination surface. However, Herrera describes that the pictures are broken into rectangles and these rectangles are mapped to the destination picture (Col. 16, lines 19-27). Therefore, the instructions must inherently identify a rectangle of data from which to receive the principal video stream within a video stream surface, a rectangle of data from which to receive the video sub-stream within a video sub-stream surface, and a rectangle at which to output the processed data within a destination surface.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsens so that the instructions identify a rectangle of data from which to receive the principal video stream within a video stream surface, a rectangle of data from which to receive the video sub-stream within a video sub-stream surface, and a rectangle at which to output the processed data within a destination surface as suggested by Herrera because Herrera suggests that breaking the pictures into rectangles of data makes it easier to transfer the data (Col. 15, line 64-Col. 16, line 27), and the instructions must identify

the rectangles of data from which to receive the data so that the data will be sent to the correct destination.

14. With regard to Claim 9, Salmonsens describes that the video sub-stream includes close captioned information [0137, 0181].

15. With regard to Claim 11, Salmonsens describes an apparatus for processing video data, comprising a renderer module (514, Figure 5) [0098]; a data processing module (214, Figure 2); and an interface module (210) that couples the renderer module to the data processing module [0033], wherein the renderer module includes logic configured to generate and provide instructions to the data processing module to execute at least the following functions: a) performing an operation on a received principal video stream [0104]; and b) combining the received principal video stream with a video sub-stream [0181].

However, Salmonsens does not teach that the performing and the combining are performed in a single stage. However, Herrera describes the performing and the combining are performed in a single stage (14, Figure 1; Col. 2, line 39-Col. 3, line 19), as discussed in the rejection for Claim 1.

16. With regard to Claim 12, Claim 12 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

17. With regard to Claim 13, Claim 13 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

18. With regard to Claim 14, Claim 14 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

19. With regard to Claim 15, Claim 15 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

20. With regard to Claim 16, Claim 16 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

21. With regard to Claim 17, Claim 17 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

22. With regard to Claim 18, Claim 18 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

23. With regard to Claim 19, Claim 19 is similar in scope to Claim 9, and therefore is rejected under the same rationale.

24. With regard to Claim 20, Claim 20 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

25. With regard to Claim 21, Salmonsens does not teach that the data processing module comprises a graphics processing module. However, Herrera describes that the data processing module comprises a graphics processing module (92, Figure 4; Col. 10, lines 59-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsens so that the data processing module comprises a graphics processing module as suggested by Herrera. Graphics processing units (GPU) are well-known in the art and are widely used. GPUs have the advantage of offloading computationally intensive transfer and lighting calculations from the CPU to the GPU, allowing faster graphics processing speeds. This means all scenes increase in detail and complexity without sacrificing performance. The advantages of GPUs can be found in many publications, such as Nvidia's website.

26. With regard to Claim 22, Salmonsens does not teach that the graphics processing module is configured to execute video processing tasks using a graphics pipeline. However, Herrera describes that the graphics processing module (92, Figure 4) is configured to execute video processing tasks using a graphics pipeline (200, Figure 5; Col. 11, lines 18-36).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsens so that the graphics processing module is configured to execute video processing tasks using a graphics pipeline as suggested by Herrera.

Graphics pipelines are well-known in the art and are commonly implemented in graphics hardware to get interactive speeds. Graphics pipelines are discussed in many publications, such as Mann's website.

27. With regard to Claim 25, Salmonsens describes an apparatus for processing video data, comprising a memory (216, Figure 2); a computer processing module for controlling the apparatus, the computer processing module being coupled to the memory [0042]; a renderer module (514, Figure 5) [0098]; a data processing module (214, Figure 2) coupled to the same memory as the computer processing module; and an interface module (210) that couples the renderer module to the data processing module [0033], wherein the renderer module includes logic configured to generate and provide instructions to the data processing module to execute at least the following functions: a) performing an operation on a received principal video stream [0104]; and b) combining the received principal video stream with a video sub-stream [0181], wherein the data processing module includes logic configured to receive the instructions, and in response thereto, execute the performing and the combining [0033].

However, Salmonsens does not teach that the data processing module comprises a graphics module and that the performing and the combining are performed in a single stage. However, Herrera describes that the data processing module comprises a graphics module, as discussed in the rejection for Claim 21 and that the performing and the combining are performed in a single stage, as discussed in the rejection for Claim 1.

28. With regard to Claim 26, Claim 26 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

29. With regard to Claim 27, Claim 27 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

30. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsens (US 20040054689A1) in view of Herrera (US006208350B1), further in view of MacInnis (US006573905B1).

Salmonsens and Herrera are relied upon for the teachings as discussed above relative to Claim 1.

However, Salmonsens and Herrera do not teach that the performing and the combining are performed on an apparatus that uses a Uniform Memory Architecture (UMA) design. However, MacInnis describes performing an operation on the principal video stream (Col. 63, lines 40-51) and combining the principal video stream with the video sub-stream, which includes close captioned information (Col. 83, lines 1-5), to produce processed data in a YUV color space (Col. 5, lines 64-67; Col. 7, lines 3-10), and outputting the processed data. MacInnis also describes that the performing and the combining are performed on an apparatus that uses a Uniform Memory Architecture (UMA) design (Col. 64, lines 14-27).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsens and Herrera so that the performing and the combining are performed on an apparatus that uses a Uniform Memory Architecture (UMA)

design as suggested by MacInnis because MacInnis suggests the advantage of facilitating substantial cost savings at the system level by allowing the CPU and other functions to utilize this memory at the same time that the memory is being used for graphics functions and display (Col. 64, lines 21-27).

31. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsens (US 20040054689A1) in view of Herrera (US006208350B1), further in view of Watson (US006466226B1).

32. With regard to Claim 23, Salmonsens and Herrera are relied upon for the teachings as discussed above relative to Claim 11.

However, Salmonsens and Herrera do not teach that the data processing module includes multiple texturing units, wherein a first texturing unit is allocated to a component of the received video stream, and a second texturing unit is allocated to the received video sub-stream. However, Watson describes that the data processing module includes multiple texturing units, wherein a first texturing unit (213, Figure 3) is allocated to a component of the received video stream, and a second texturing unit (215) is allocated to the received video sub-stream (Col. 6, line 66-Col. 7, line 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsens and Herrera so that the data processing module includes multiple texturing units, wherein a first texturing unit is allocated to a component of the received video stream, and a second texturing unit is allocated to the received video sub-stream

as suggested by Watson because Watson suggests the advantage of being able to process the texturing for the video stream and the texturing for the video sub-stream at the same time if needed (Col. 6, line 66-Col. 7, line 15).

33. With regard to Claim 24, Salmonsens and Herrera do not teach that the data processing module is configured to execute the performing and the combining in a single stage by processing video data obtained from the first and second texturing units substantially in parallel. However, Watson describes that the first and second texturing units can be processed at the same time or substantially in parallel (Col. 6, line 66-Col. 7, line 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsens and Herrera so that the data processing module is configured to execute the performing and the combining in a single stage by processing video data obtained from the first and second texturing units substantially in parallel as suggested by Watson. Parallel processing is well-known in the art and widely used. Parallel processing allows two processors to operate simultaneously to speed processing. This can be found in many publications, such as the definitions of parallel processing found by Google.

Prior Art of Record

“YUV,” available at <http://en.wikipedia.org/wiki/YUV>.

“GPU: Changes Everything,” available at <http://www.nvidia.com/object/gpu.html>.

Stephen Mann, “The Graphics Rendering Pipeline,” 1997, available at
<http://medialab.di.unipi.it/web/IUM/Waterloo/node7.html>.

“Parallel Processing,” available at
<<http://www.google.com/search?hl=en&lr=&oi=define&q=define:parallel+processing>>.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

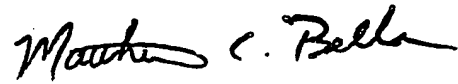
If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, reading "Matthew C. Bella". The signature is written in a cursive style with a large, stylized "M" and "B".

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600